DESCRIPTION

The PT2315E is an audio processor designed for versatile application, includes master volume control with low frequency loudness compensation, speaker output attenuator and tone control. It is a good solution for the home audio signal processing.

Due to the high reliability requirement from the audio business, the PT2315E improves both audio performances and input surge current capability, these causes the PT2315E is the best solution for the cost-effective audio systems.

APPLICATIONS

- Flat Panel TV
- Home Audio System
- Powered Speaker System
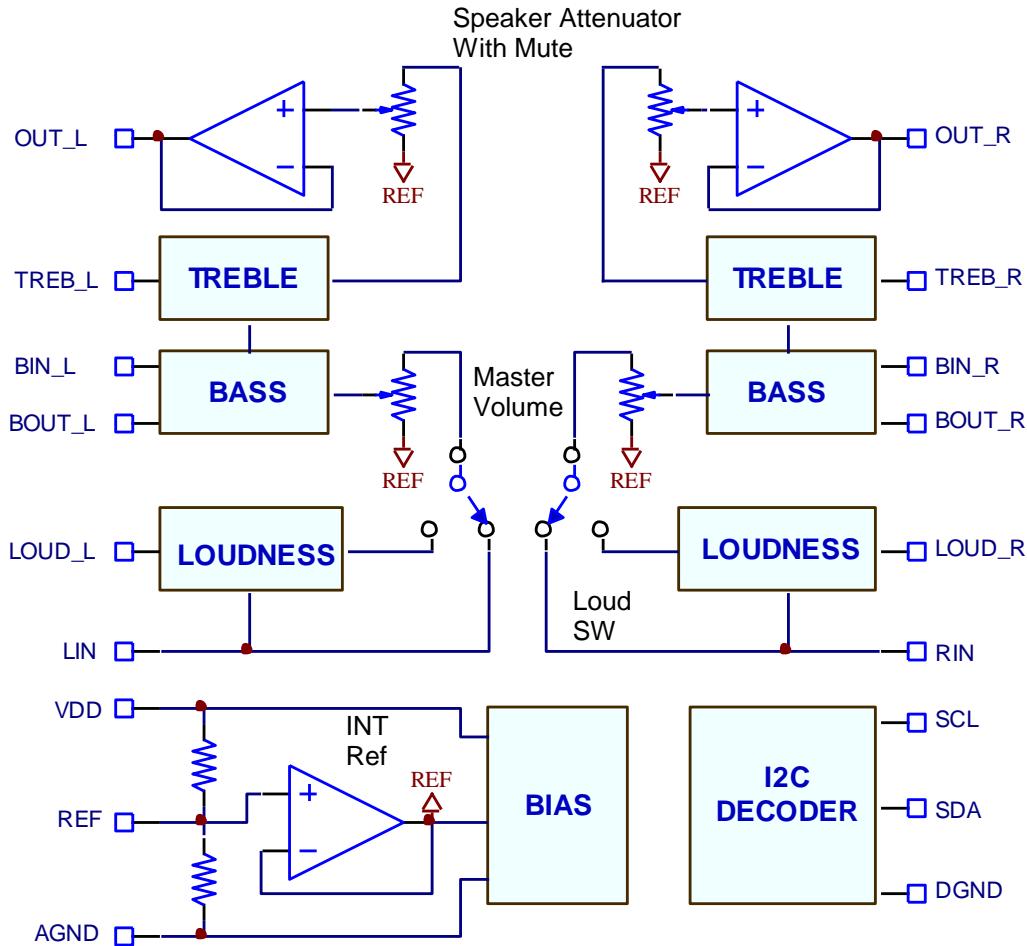
FEATURES

- Master volume from 0 dB to -78.75dB in 1.25dB/step
- Speaker attenuator for balance, range from 0dB to -38.75dB in 1.25dB/step
- Each channel output can be muted individually.
- Low frequency loudness compensation
- Bass and Treble control, range from -14dB to +14dB in 2dB/step
- Wide operation range (VDD=4V to 10V)
- Low harmonic distortion, low noise
- Improved and replace PT2315 and PT2315A

BLOCK DIAGRAM

APPLICATION CIRCUIT

PT2315E

Pin	Left side		Right side	Pin
1	REF		SCL	20
2	VDD		SDA	19
3	AGND		DGND	18
4	TREB_L		OUT_L	17
5	TREB_R		OUT_R	16
6	RIN		BOUT_R	15
7	LOUD_R		BIN_R	14
8	NC		BOUT_L	13
9	LOUD_L		BIN_L	12
10	NC		LIN	11

VDD
22uF
2.7n
2.7n
100n
100n
100n

MCU

10uF
10uF
100n   5.6K
100n
100n   5.6K
100n

Power
Amplifier

Left

Right

**Input Surge
Protection**

AUDIO 1
L
R
2.2K
2.2K
2.2uF
2.2uF
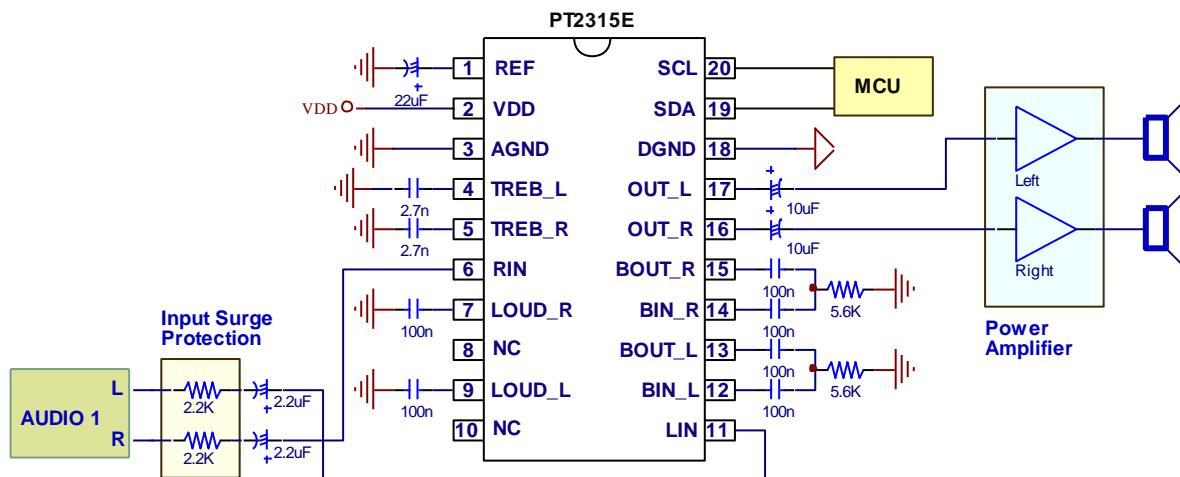
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2315E-S	20 Pins, SOP, 300mil	PT2315E

PIN CONFIGURATION

REF	1	20 SCL
VDD	2	19 SDA
AGND	3	18 DGND
TREB_L	4	17 OUT_L
TREB_R	5	16 OUT_R
RIN	6	15 BOUT_R
LOUD_R	7	14 BIN_R
NC	8	13 BOUT_L
LOUD_L	9	12 BIN_L
NC	10	11 LIN

PT2315E
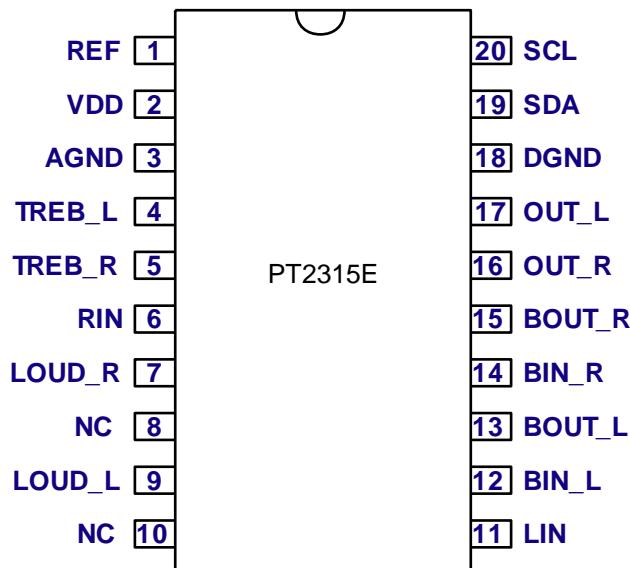
PIN DESCRIPTION

| Pin Name	I/O	Description	Pin No.
REF	-	Analog reference voltage (1/2VDD)	1
VDD	-	Supply input voltage	2
AGND	-	Analog ground	3
TREB_L	I	Left channel input for treble controller	4
TREB_R	I	Right channel input for treble controller	5
RIN	I	Right channel volume controller input	6
LOUD_R	I	Right channel loudness input	7
NC		No connect	8
LOUD_L	I	Left channel loudness input	9
NC		No connect	10
LIN	I	Left channel volume controller input	11
BIN_L	I	Left channel input for bass controller	12
BOUT_L	O	Left channel output for bass controller	13
BIN_R	I	Right channel input for bass controller	14
BOUT_R	O	Right channel output for bass controller	15
OUT_R	O	Right rear speaker output	16
OUT_L	O	Left rear speaker output	17
DGND	-	Digital ground	18
SDA	I	I²C data input	19
SCL	I	I²C clock input	20

CONTROL BUS SPECIFICATION

BUS INTERFACE

All functions of the PT2315E are controlled by the I²C interface, the interface is consisting by SDA and SCL pins. Detail protocol of the I²C bus will discuss on the next section. It should be noted that the bus level pull-up resistors connected to the PT2315E positive supply voltage may required in some application especially the MCU output high level is no enough.

DATA VALIDITY

A data on the SDA Line is considered valid and stable only when the SCL Signal is in HIGH State. The HIGH and LOW State of the SDA Line can only change when the SCL signal is LOW. Please refer to the figure below.
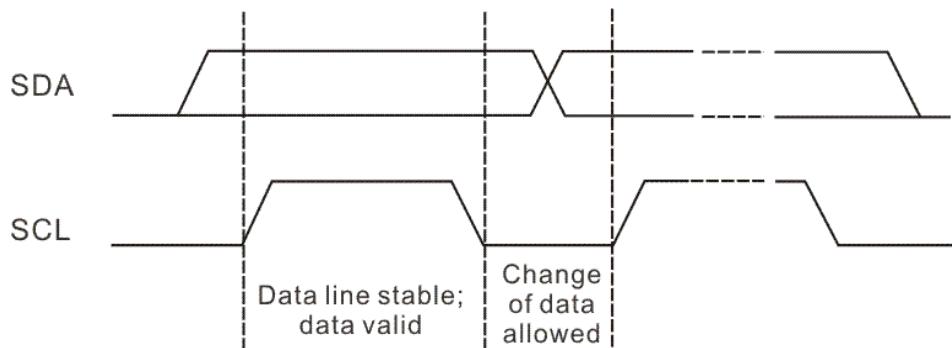

START AND STOP CONDITIONS

A Start Condition is activated when
    1) The SCL is set to HIGH and
    2) SDA shifts from HIGH to LOW State.

The Stop Condition is activated when
    1) SCL is set to HIGH and
    2) SDA shifts from LOW to HIGH State. Please refer to the timing diagram below.
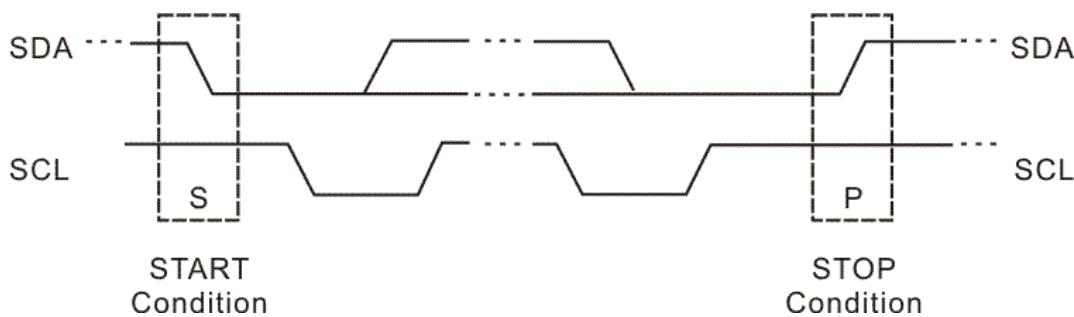

BYTE FORMAT

Every byte transmitted to the SDA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is first transmitted.

ACKNOWLEDGE

During the Acknowledge clock pulse (ACK), the SDA output port of the master device (μP) would be sets on Hi-Z state, if peripheral device (ex : audio processor) recognize the I²C command the SDA line will be pull-down by slave device during the SCL clock pulse held in HIGH state period. Please refer to the diagram below. The slave device that has been addressed to generate an Acknowledge after receiving each byte, otherwise, the SDA Line will remain at the High level in period of the ninth (9th) clock pulse. In this case, the host controller will generate a STOP sign in order to abort the transfer mission.
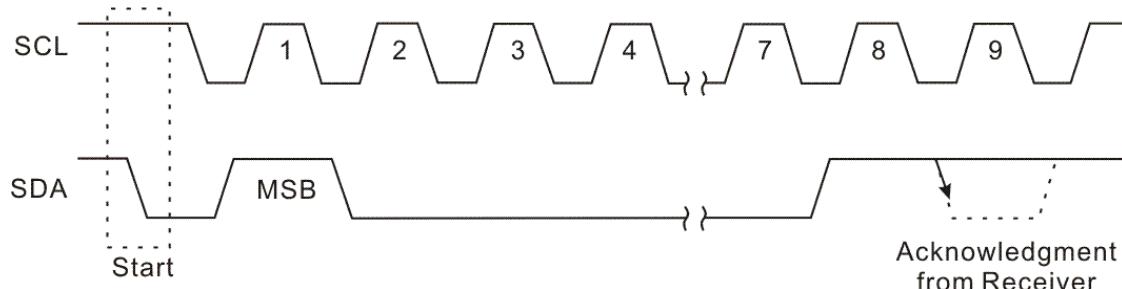

TRANSMISSION WITHOUT ACKNOWLEDGE

If the application does not need to verify the Acknowledge signal that generated by the slave device is right or not, host controller can just bypass the acknowledge check and transmit next data byte to the slave device. If this approach is used, there are greater chances of faulty operation as well as decrease in noise immunity.

INTERFACE PROTOCOL

The interface protocol sequence was defined in below section:
- A Start sign.
- A Chip Address of the desire slave device. The W Bit must be "**0**" (written). The PT2315E will always response an Acknowledge on the end of each byte.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition

ACK=Acknowledge

PT2315E CHIP ADDRESS

The PT2315E chip address is 88H AND binary table is shown on below.

MSB							LSB
1	0	0	0	1	0	0	0

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Master Volume
1	0	0	B1	B0	A2	A1	A0	Speaker ATT L
1	0	1	B1	B0	A2	A1	A0	Speaker ATT R
0	1	0	x	x	LD	x	x	Loudness
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

x=don't care.

DATA RATE

The PT2315E support Standard-Mode (100kbit/s) I²C data rate In all operation condition, in specified condition it also support Fast-Mode (400kbit/s) I²C data rate, please refer to the follow table:

MCU Level	PT2315E VDD Voltage						
	4V	5V	6V	7V	8V	9V	10V
2.5V	F	F	x	x	x	x	X
3.3V	F	F	F	F	S	S	X
5V	x	F	F	F	F	F	F

Note 1 : x=Not allow in this combination, S=Standard Mode Supported, F=Fast Mode Supported.
Note 2 : Data rate specification is design guarantee only, not fully tested in every combination.

I²C BUS INITIAL TIME

The PT2315E is controlled by the I²C bus command; each time the supply voltage applied to chip it needs an initial time to reset all of the internal decoder register, in this period access the I²C bus is prohibited. The initial time is determinate by capacitance it attached on REF pin (CREF) and Td. For proper operation USER must check the I²C starts timing is fit this requirement and recommended Td timing shown on next page is 50mS.
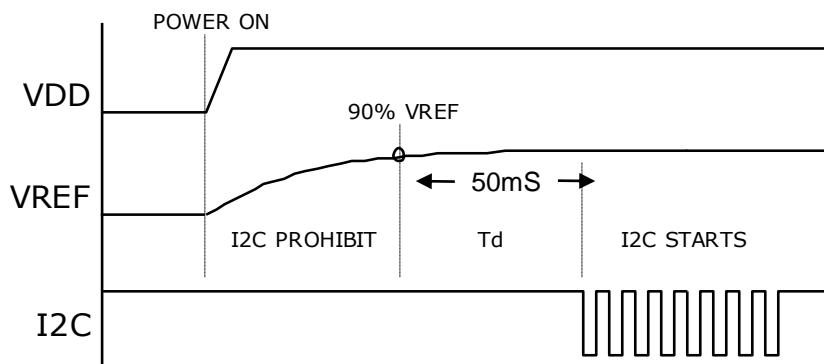
FUNCTIONAL DESCRIPTION

MASTER VOLUME

The table below gives a detailed description of the Master Volume Data Bytes. For example, a volume of -37.5dB is given by 0 0 0 1 1 1 1 0.

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	1.25dB step
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	10dB step
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

SPEAKER ATTENUATORS

The speaker attenuator in most audio system is as channel balance function, the table below gives a detailed description of the speaker attenuators data bytes. Total control range of the speaker attenuator is from 0dB to -37.5dB.

Example 1, an attenuation gain of -6.25dB on the Speaker Right channel is combined 0dB and -6.25dB, therefore it should given by : 1 01 0 0 1 0 1.

Example 2, an attenuation gain of -32.5dB on the Speaker Left channel is combined -30dB and -2.5dB, therefore it should given by : 1 0 0 1 1 0 1 0.

MSB							LSB	Function
1	0	0	B1	B0	A2	A1	A0	Speaker L
1	0	1	B1	B0	A2	A1	A0	Speaker R
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
		0	0					0
		0	1					-10
		1	0					-20
		1	1					-30
		1	1	1	1	1	1	Mute

LOUDNESS

| MSB							LSB	Function
0	1	0	x	x	LD	x	x	Loudness
					0			ON
					1			OFF

Note: x=don't care.

BASS AND TREBLE DATA BYTES

The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at -12dB is given by: 0 1 1 1 0 0 0 1 (0x71).

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6 dB
				0	1	0	1	-4 dB
				0	1	1	0	-2 dB
				0	1	1	1	0 dB
				1	1	1	1	0 dB
				1	1	1	0	+2 dB
				1	1	0	1	+4 dB
				1	1	0	0	+6 dB
				1	0	1	1	+8 dB
				1	0	1	0	+10 dB
				1	0	0	1	+12 dB
				1	0	0	0	+14 dB

TUNNING TONE CURVE CHARACTERISTCS

The tone control response character is possible tuned to match user's wishes, please refer to following chart to realize the characteristics between the different component values.

For the reasons to achieve low distortion and precision response gain, using high quality low tolerance X7R SMD capacitor on tone circuit is recommended.

The loudness boost gain is adaptive with the master volume attenuation setting, more attenuation means more low frequency boost, in the maximum volume the loudness boost will return to flat response.
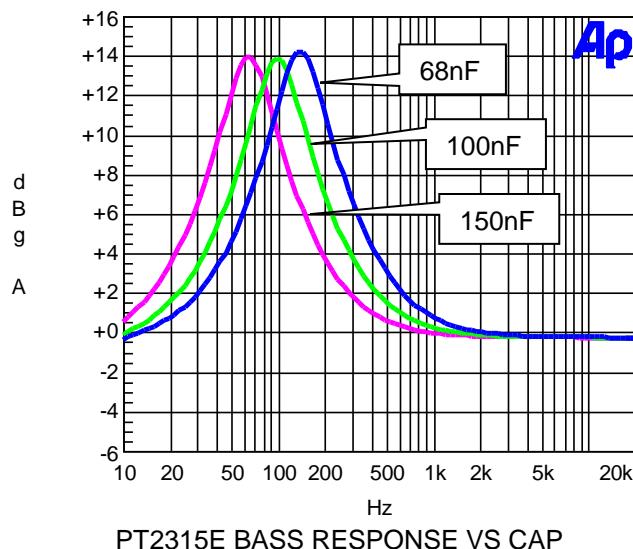
PT2315E BASS RESPONSE VS CAP
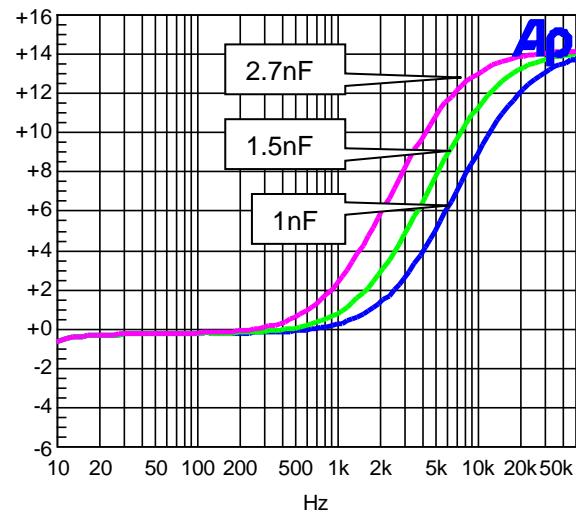
PT2315E TREBLE RESPONSE VS CAP
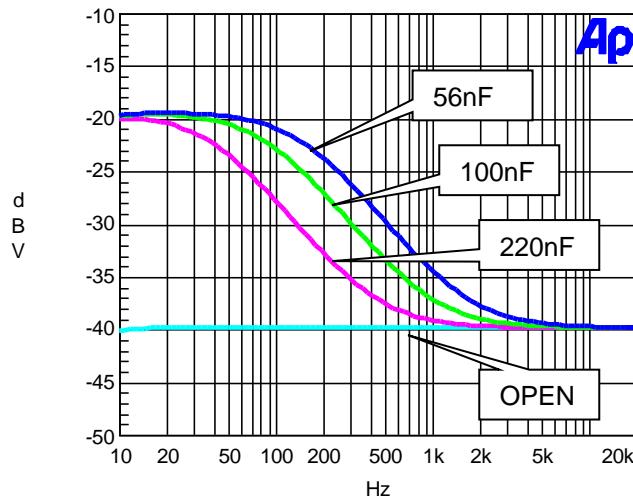
PT2315E LOUDNESS RESPONSE VS CAP
(VOLUME=-40dB)
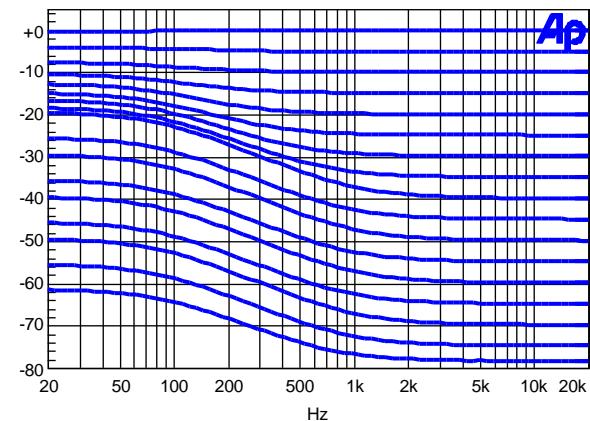
PT2315E LOUDNESS RESPONSE VS MASTER
VOLUME

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min.	Max.	Unit
Operating supply voltage		VDD	-	10	V
Input latch up current		Iin	-100	+100	mA
ESD grade	Human body model	HBM	-2	+2	KV
	Machine model	MM	-0.2	+0.2	KV
Input voltage		Vin	-0.3	VDD+0.3	V
Operating temperature		Topr	-40	+85	℃
Storage temperature		Tstg	-65	+150	℃

QUICK REFERENCE DATA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	4	9	10	V
Max. input signal handling	V$_{CL}$	2.3	2.6	-	Vrms
Total harmonic distortion (1Vrms,1KHz)	THD	-	0.03	0.07	%
Signal to noise ratio	S/N	-	100	-	dBV
Channel separation (f=1KHz)	Sc	-	100	-	dB
Volume control 1.25dB step		-78.75	-	0	dB
Bass & treble control 2dB step		-14	-	+14	dB
Balance control 1.25dB step		-37.5	-	0	dB
Input gain 3.75dB step		0	-	11.25	dB
Mute attenuation		-	100	-	dB

# ELECTRICAL CHARACTERISTICS

Unless otherwise specified: Ta=25℃, VDD=9V, RL=10KΩ, Rg=20Ω, all controls flat, F=1KHz, and all of peripheral components according to standard application circuit.

| Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power Supply						
Supply voltage	VDD	-	4	9	10	V
Supply current	Is	VDD=9V		30	40	mA
		VDD=5V		25	32	
Volume Control						
Input resistance	R_{IN}	LIN,RIN, VOL=0dB, LD=OFF	13	20	27	KΩ
Min. attenuation	A_{VMIN}	-	-1	0	1	dB
Max. attenuation	A_{VMAX}	-	-75	-78.75	-82	dB
Step resolution	A_{STEP}	-	1.15	1.25	1.3	dB
Attenuation set error	E_A	VOL=0~-70dB	-1	0	1	dB
Speaker Attenuators						
Max. gain	A_{VMIN}	-	-1	0	+1	dB
Max. attenuation	A_{VMAX}	-	-36	-37.5	-39	dB
Step resolution	S_{STEP}	-	1.15	1.25	1.35	dB
Attenuation set error	E_A	-	-1	0	1	dB
Output mute attenuation	A_{MUTE}	-		100		dB
DC offset	V_{DCO}	0dB to MUTE		5	10	mV
Bass Control						
Control range	Gb	Max. Boost/Cut	±12	±14	±16	dB
Step resolution	B_{STEP}	-	1.7	2	2.3	dB
Feedback resistance	R_B	-	34	44	58	KΩ
Treble Control						
Control range	Gt	Max. Boost/Cut	±12	±14	±16	dB
Step resolution	T_{STEP}	-	1.7	2	2.3	dB
Loudness Control						
Boost gain	G_{LD}	Volume=-40dB, F=20Hz	18	20	22	dB
Audio Outputs						
Max. output level	V_{OMAX}	THD=1%	2.3	2.6		Vrms
DC voltage level	V_{OUT}	-	0.49	0.5	0.51	VDD
Minimum Load	RL	OUT_L,OUT_R	5			KΩ
General						
Signal to noise ratio	SNR	All Gain=0dB, A-weighted		100		dBV
		All Gains=0dB, Muted		100		
Distortion	THD	All Gain=0, Vin=1Vrms		0.03	0.07	%
		All Gain=0, Vin=100Vrms		0.01	0.03	
Channel separation	Cs	L to R or R to L channel	90	100		dB
I²C crosstalk	Ct	I²C to audio output		90		dB
Ripple rejection	PSRR	CREF=22μF, F=100Hz		75		dB
I²C Bus						
Input low voltage	V_{IL}	VDD=9V			1	V
Input high voltage	V_{IH}	VDD=9V	3			V
Input current	I_{IN}	-	-5		+5	μA
SDA pull down voltage	Vack	Rpull up=3K, ACK=Active		0.4		V

BASS RESPONSE

TREBLE RESPONSE

2 CHANNEL CROSSTALK

PSRR

Cref=22μF

OUTPUT THD VS VDD VOLTAGE

4V	
5V	
8V	
9V	
10V	
(RL=10KΩ)	

Princeton Technology Corp.

普 誠 科 技
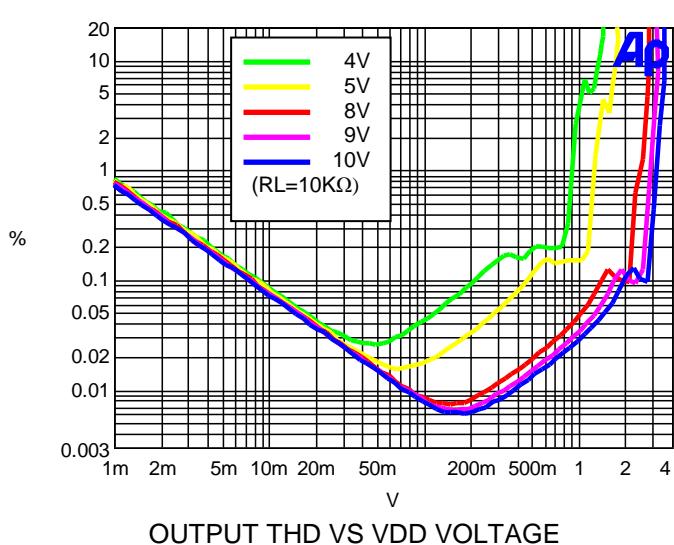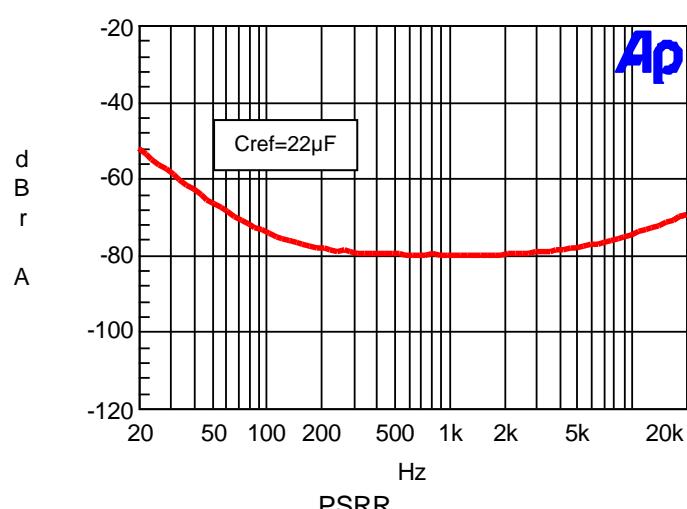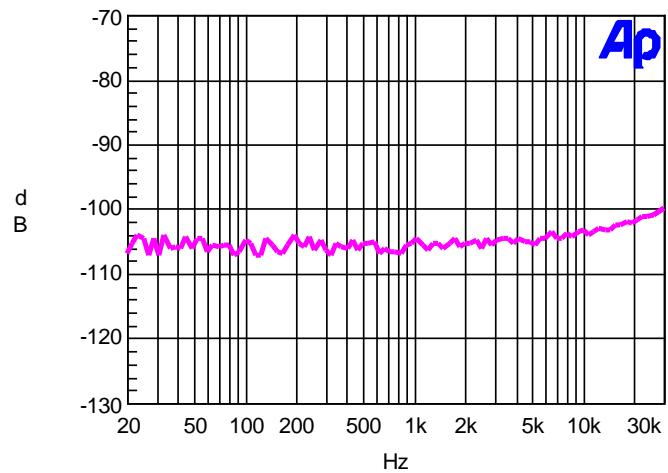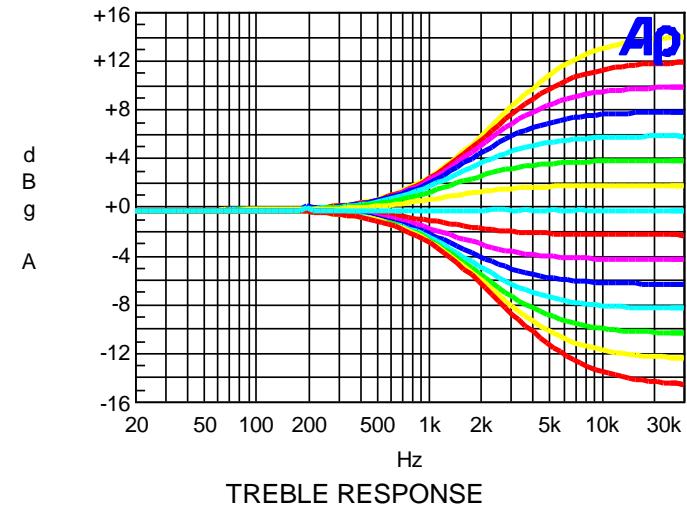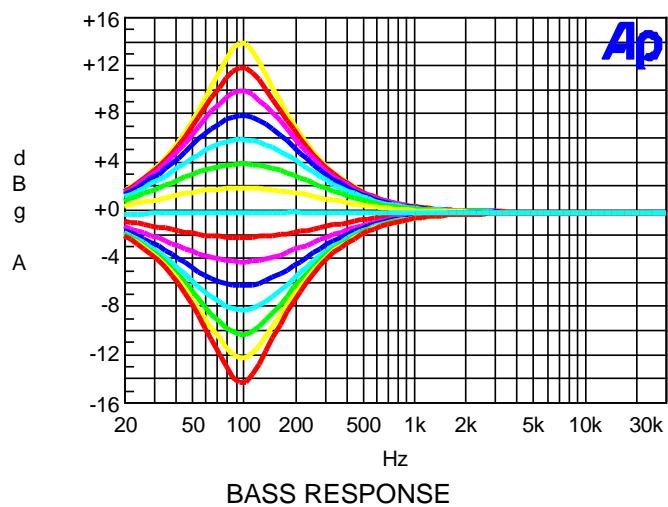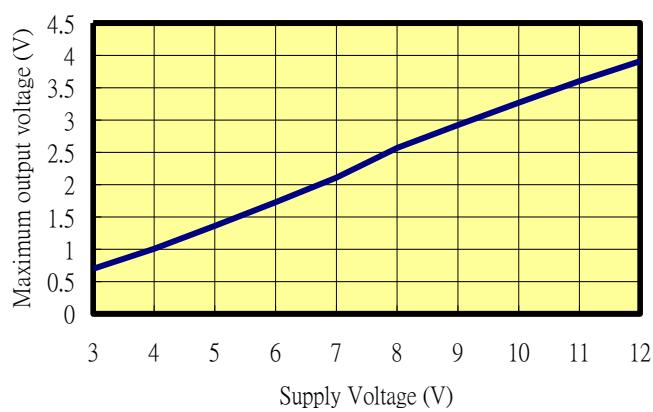
MAXIMUM OUTPUT LEVEL (RL=100KΩ)
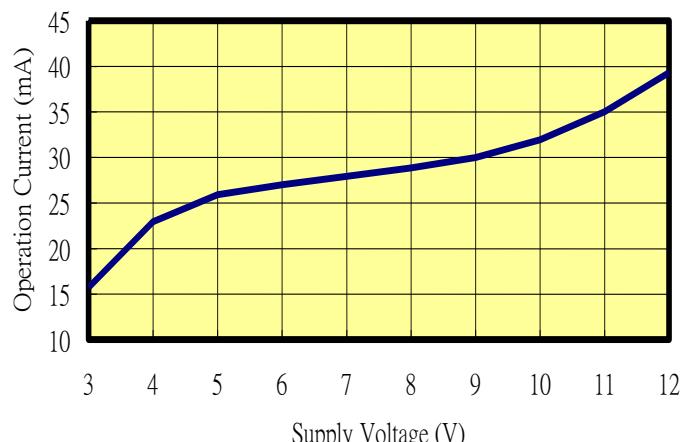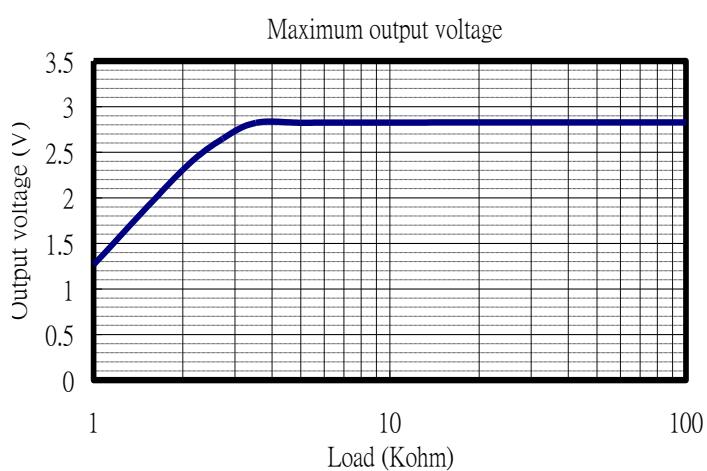
MAXIMUM OUTPUT LEVEL VS R_LOAD

VOLUME ATTENUATION

SUPPLY CURRENT VS VDD
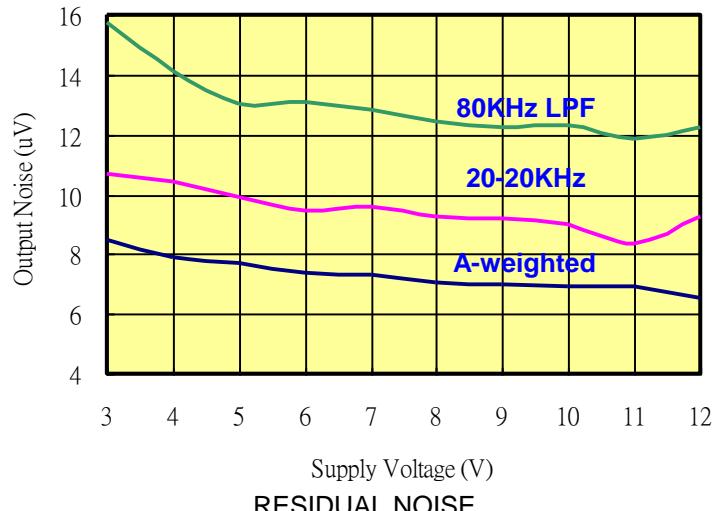
RESIDUAL NOISE
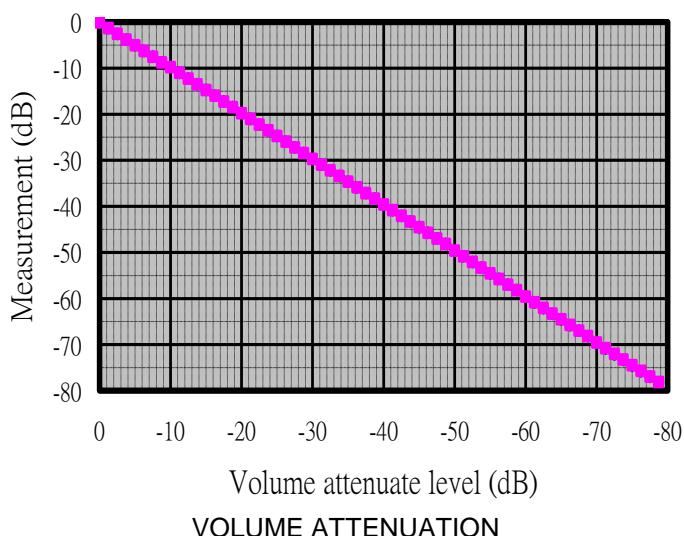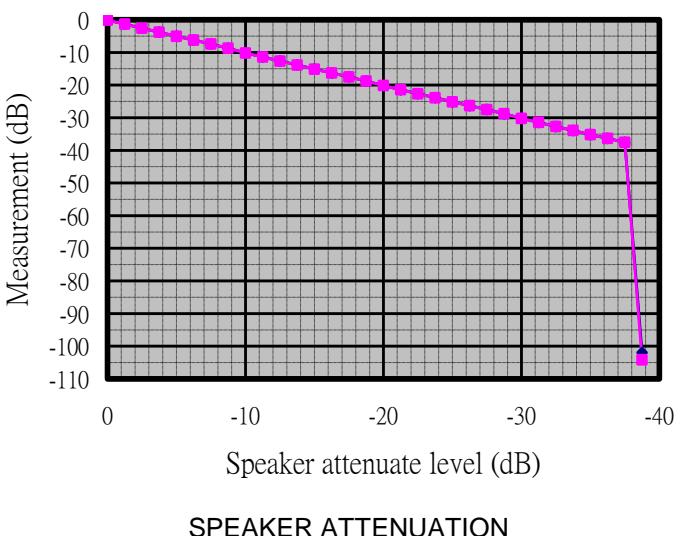
SPEAKER ATTENUATION

PACKAGE INFORMATION

20 PINS, SOP, 300MIL

PIN 1 INDENT
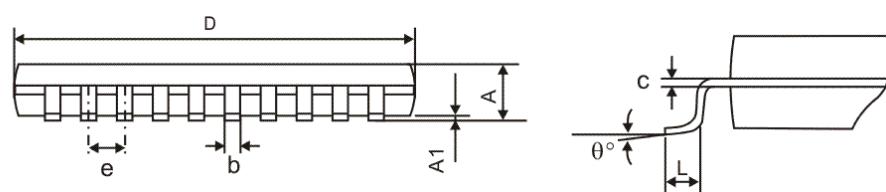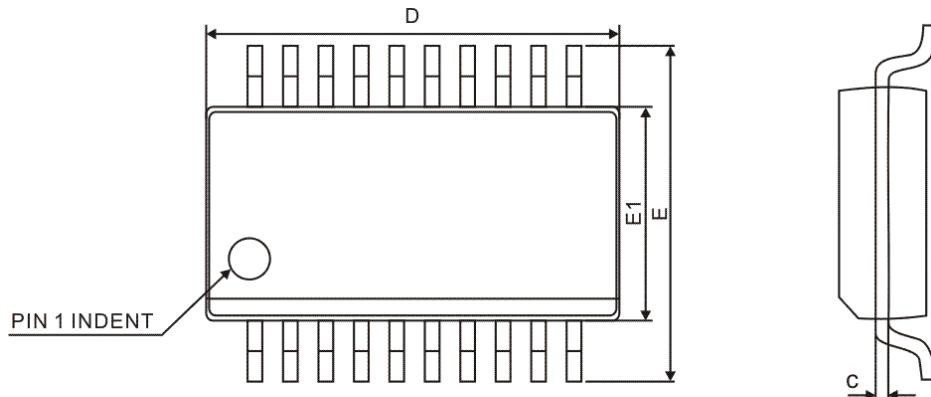
Symbol	Dimensions(mm)		
	Min.	**Nom.**	**Max.**
A	-	-	2.65
A1	0.10	-	0.30
b	0.31	-	0.51
c	0.20	-	0.33
e	1.27 BSC		
D	12.80 BSC		
E	10.30 BSC		
E1	7.50 BSC		
L	0.40	-	1.27
θ	0°	-	8°

Note: Refer to JEDEC MS-013AC

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian, Dist., New Taipei City 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw