

Pulse Width Modulator Control Circuit

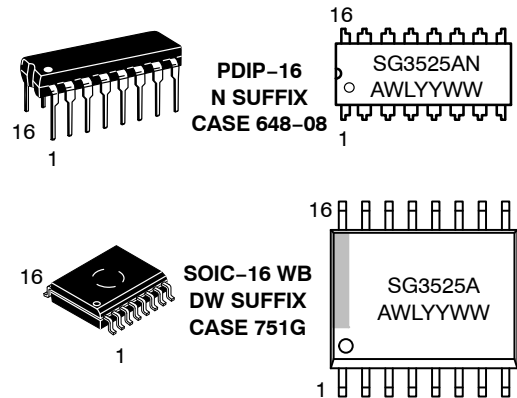
SG3525A

The SG3525A pulse width modulator control circuit offers improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on-chip +5.1 V reference is trimmed to $\pm 1\%$ and the error amplifier has an input common-mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of deadtime can be programmed by a single resistor connected between the C_T and Discharge pins. This device also features built-in soft-start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft-start capacitor when V_{CC} is below nominal. The output stages are totem-pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG3525A features NOR logic resulting in a low output for an off-state.

Features

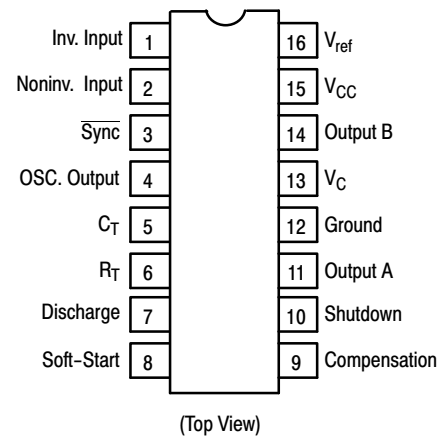
- 8.0 V to 35 V Operation
- 5.1 V $\pm 1.0\%$ Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Deadtime Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse-by-Pulse Shutdown
- Dual Source/Sink Outputs: ± 400 mA Peak
- Pb-Free Packages are Available*

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDETRM/D.

SG3525A

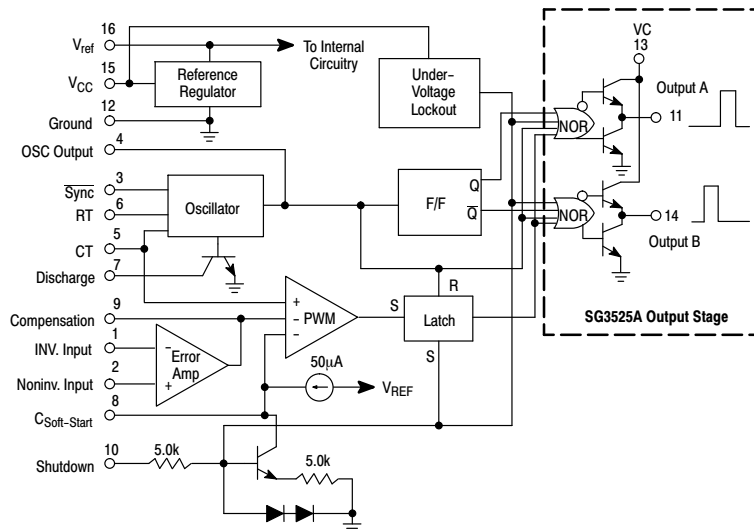


Figure 1. Representative Block Diagram

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|--------------|-------------------------|-----------------------|
| SG3525ANG | PDIP-16 (Pb-Free) | 25 Units / Rail |
| SG3525ADWR2G | SOIC-16 WB (Pb-Free) | 1000 Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|-----------------|------------------|---------------------------|
| Supply Voltage | V_{CC} | +40 | Vdc |
| Collector Supply Voltage | V_C | +40 | Vdc |
| Logic Inputs | | -0.3 to +5.5 | V |
| Analog Inputs | | -0.3 to V_{CC} | V |
| Output Current, Source or Sink | I_O | ±500 | mA |
| Reference Output Current | I_{ref} | 50 | mA |
| Oscillator Charging Current | | 5.0 | mA |
| Power Dissipation $T_A = +25^\circ\text{C}$ (Note 1) $T_C = +25^\circ\text{C}$ (Note 2) | P_D | 1000 2000 | mW |
| Thermal Resistance, Junction-to-Air | $R_{\theta JA}$ | 100 | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 60 | $^\circ\text{C}/\text{W}$ |
| Operating Junction Temperature | T_J | +150 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -55 to +125 | $^\circ\text{C}$ |
| Lead Temperature (Soldering, 10 seconds) | T_{Solder} | +300 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Derate at 10 mW/ $^\circ\text{C}$ for ambient temperatures above +50 $^\circ\text{C}$.
2. Derate at 16 mW/ $^\circ\text{C}$ for case temperatures above +25 $^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS

| Characteristics | Symbol | Min | Max | Unit |
|--|-----------|--------|--------------|------------------|
| Supply Voltage | V_{CC} | 8.0 | 35 | Vdc |
| Collector Supply Voltage | V_C | 4.5 | 35 | Vdc |
| Output Sink/Source Current (Steady State) (Peak) | I_O | 0 0 | ±100 ±400 | mA |
| Reference Load Current | I_{ref} | 0 | 20 | mA |
| Oscillator Frequency Range | f_{osc} | 0.1 | 400 | kHz |
| Oscillator Timing Resistor | R_T | 2.0 | 150 | k Ω |
| Oscillator Timing Capacitor | C_T | 0.001 | 0.2 | μF |
| Deadtime Resistor Range | R_D | 0 | 500 | Ω |
| Operating Ambient Temperature Range | T_A | 0 | +70 | $^\circ\text{C}$ |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

APPLICATION INFORMATION

Shutdown Options (See Block Diagram, page 2)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM

latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

SG3525A

ELECTRICAL CHARACTERISTICS ($V_{CC} = +20$ Vdc, $T_A = T_{low}$ to T_{high} [Note 3], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---------------------------|------|------|------|---------------------|
| REFERENCE SECTION | | | | | |
| Reference Output Voltage ($T_J = +25^\circ\text{C}$) | V_{ref} | 5.00 | 5.10 | 5.20 | Vdc |
| Line Regulation ($+8.0\text{ V} \leq V_{CC} \leq +35\text{ V}$) | Reg_{line} | – | 10 | 20 | mV |
| Load Regulation ($0\text{ mA} \leq I_L \leq 20\text{ mA}$) | Reg_{load} | – | 20 | 50 | mV |
| Temperature Stability | $\Delta V_{ref}/\Delta T$ | – | 20 | – | mV |
| Total Output Variation Includes Line and Load Regulation over Temperature | ΔV_{ref} | 4.95 | – | 5.25 | Vdc |
| Short Circuit Current ($V_{ref} = 0\text{ V}$, $T_J = +25^\circ\text{C}$) | I_{SC} | – | 80 | 100 | mA |
| Output Noise Voltage ($10\text{ Hz} \leq f \leq 10\text{ kHz}$, $T_J = +25^\circ\text{C}$) | V_n | – | 40 | 200 | μV_{rms} |
| Long Term Stability ($T_J = +125^\circ\text{C}$) (Note 4) | S | – | 20 | 50 | mV/khr |

OSCILLATOR SECTION (Note 5, unless otherwise noted.)

| | | | | | |
|---|----------------------------------|-----|-----------|-----------|---------------|
| Initial Accuracy ($T_J = +25^\circ\text{C}$) | | – | ± 2.0 | ± 6.0 | % |
| Frequency Stability with Voltage ($+8.0\text{ V} \leq V_{CC} \leq +35\text{ V}$) | $\frac{\Delta f_{osc}}{DV_{CC}}$ | – | ± 1.0 | ± 2.0 | % |
| Frequency Stability with Temperature | $\frac{\Delta f_{osc}}{DT}$ | – | ± 0.3 | – | % |
| Minimum Frequency ($R_T = 150\text{ k}\Omega$, $C_T = 0.2\text{ }\mu\text{F}$) | f_{min} | – | 50 | – | Hz |
| Maximum Frequency ($R_T = 2.0\text{ k}\Omega$, $C_T = 1.0\text{ nF}$) | f_{max} | 400 | – | – | kHz |
| Current Mirror ($I_{RT} = 2.0\text{ mA}$) | | 1.7 | 2.0 | 2.2 | mA |
| Clock Amplitude | | 3.0 | 3.5 | – | V |
| Clock Width ($T_J = +25^\circ\text{C}$) | | 0.3 | 0.5 | 1.0 | μs |
| Sync Threshold | | 1.2 | 2.0 | 2.8 | V |
| Sync Input Current (Sync Voltage = $+3.5\text{ V}$) | | – | 1.0 | 2.5 | mA |

ERROR AMPLIFIER SECTION ($V_{CM} = +5.1\text{ V}$)

| | | | | | |
|--|-----------|-----|-----|-----|---------------|
| Input Offset Voltage | V_{IO} | – | 2.0 | 10 | mV |
| Input Bias Current | I_{IB} | – | 1.0 | 10 | μA |
| Input Offset Current | I_{IO} | – | – | 1.0 | μA |
| DC Open Loop Gain ($R_L \geq 10\text{ M}\Omega$) | A_{VOL} | 60 | 75 | – | dB |
| Low Level Output Voltage | V_{OL} | – | 0.2 | 0.5 | V |
| High Level Output Voltage | V_{OH} | 3.8 | 5.6 | – | V |
| Common Mode Rejection Ratio ($+1.5\text{ V} \leq V_{CM} \leq +5.2\text{ V}$) | CMRR | 60 | 75 | – | dB |
| Power Supply Rejection Ratio ($+8.0\text{ V} \leq V_{CC} \leq +35\text{ V}$) | PSRR | 50 | 60 | – | dB |

PWM COMPARATOR SECTION

| | | | | | |
|--|------------|-----|------|-----|---------------|
| Minimum Duty Cycle | DC_{min} | – | – | 0 | % |
| Maximum Duty Cycle | DC_{max} | 45 | 49 | – | % |
| Input Threshold, Zero Duty Cycle (Note 5) | V_{th} | 0.6 | 0.9 | – | V |
| Input Threshold, Maximum Duty Cycle (Note 5) | V_{th} | – | 3.3 | 3.6 | V |
| Input Bias Current | I_{IB} | – | 0.05 | 1.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. $T_{low} = 0^\circ$ $T_{high} = +70^\circ\text{C}$

4. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

5. Tested at $f_{osc} = 40\text{ kHz}$ ($R_T = 3.6\text{ k}\Omega$, $C_T = 0.01\text{ }\mu\text{F}$, $R_D = 0\text{ }\Omega$).

ELECTRICAL CHARACTERISTICS (continued)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|----------------------|----------|------------|------------|---------------|
| SOFT-START SECTION | | | | | |
| Soft-Start Current ($V_{\text{shutdown}} = 0 \text{ V}$) | | 25 | 50 | 80 | μA |
| Soft-Start Voltage ($V_{\text{shutdown}} = 2.0 \text{ V}$) | | - | 0.4 | 0.6 | V |
| Shutdown Input Current ($V_{\text{shutdown}} = 2.5 \text{ V}$) | | - | 0.4 | 1.0 | mA |
| OUTPUT DRIVERS (Each Output, $V_{\text{CC}} = +20 \text{ V}$) | | | | | |
| Output Low Level ($I_{\text{sink}} = 20 \text{ mA}$) ($I_{\text{sink}} = 100 \text{ mA}$) | V_{OL} | - - | 0.2 1.0 | 0.4 2.0 | V |
| Output High Level ($I_{\text{source}} = 20 \text{ mA}$) ($I_{\text{source}} = 100 \text{ mA}$) | V_{OH} | 18 17 | 19 18 | - - | V |
| Under Voltage Lockout (V_8 and $V_9 = \text{High}$) | V_{UL} | 6.0 | 7.0 | 8.0 | V |
| Collector Leakage, $V_{\text{C}} = +35 \text{ V}$ (Note 6) | $I_{\text{C(leak)}}$ | - | - | 200 | μA |
| Rise Time ($C_{\text{L}} = 1.0 \text{ nF}$, $T_{\text{J}} = 25^\circ\text{C}$) | t_{r} | - | 100 | 600 | ns |
| Fall Time ($C_{\text{L}} = 1.0 \text{ nF}$, $T_{\text{J}} = 25^\circ\text{C}$) | t_{f} | - | 50 | 300 | ns |
| Shutdown Delay ($V_{\text{DS}} = +3.0 \text{ V}$, $C_{\text{S}} = 0$, $T_{\text{J}} = +25^\circ\text{C}$) | t_{ds} | - | 0.2 | 0.5 | μs |
| Supply Current ($V_{\text{CC}} = +35 \text{ V}$) | I_{CC} | - | 14 | 20 | mA |

6. Applies to SG3525A only, due to polarity of output pulses.

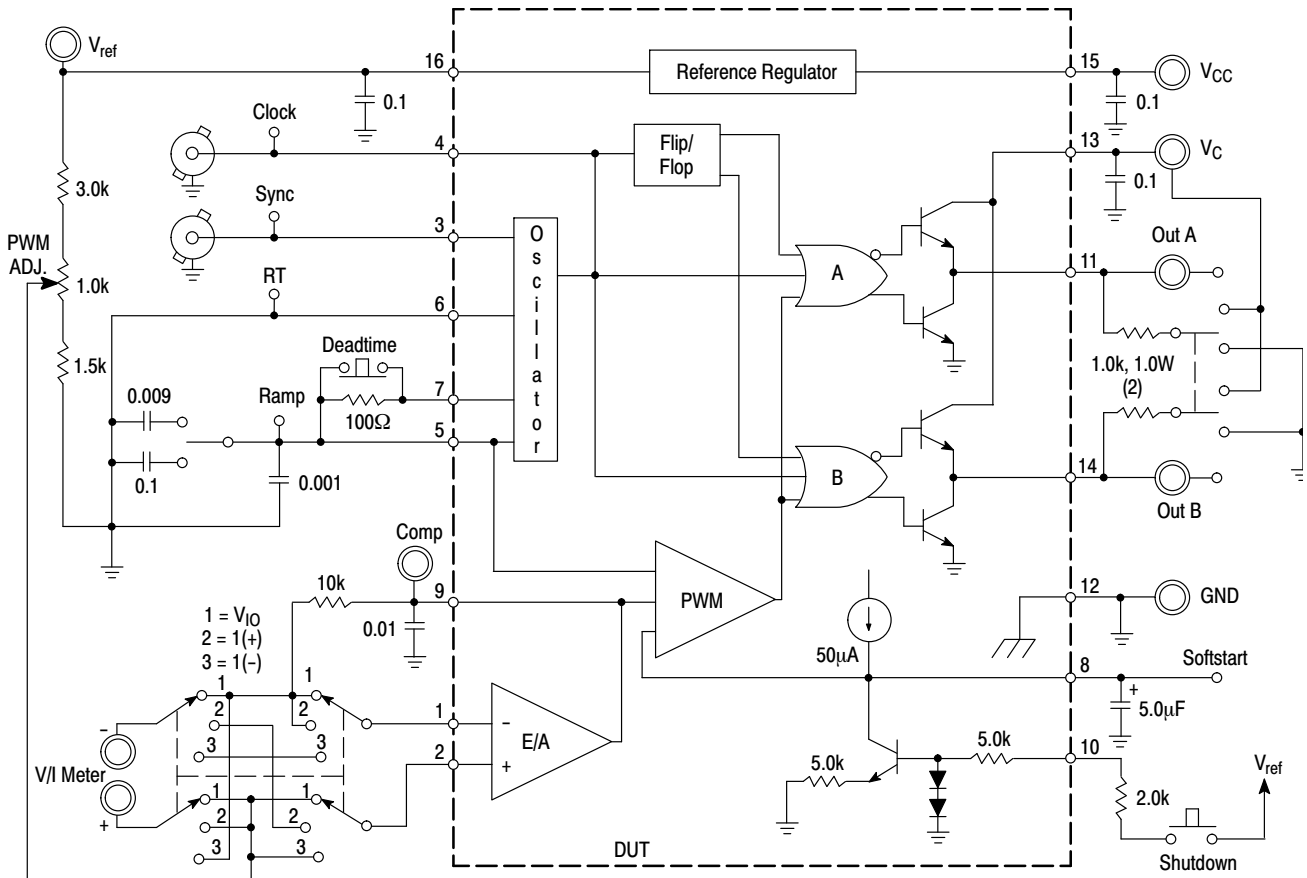


Figure 2. Lab Test Fixture

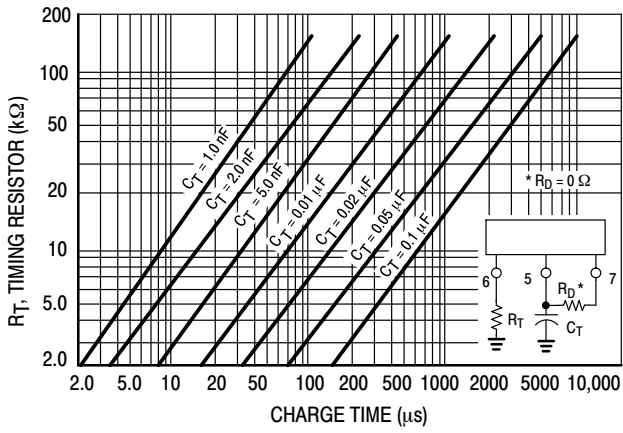


Figure 3. Oscillator Charge Time versus R_T

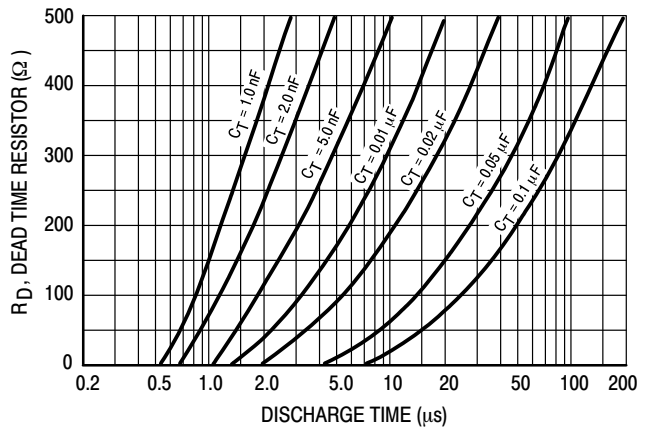


Figure 4. Oscillator Discharge Time versus R_D

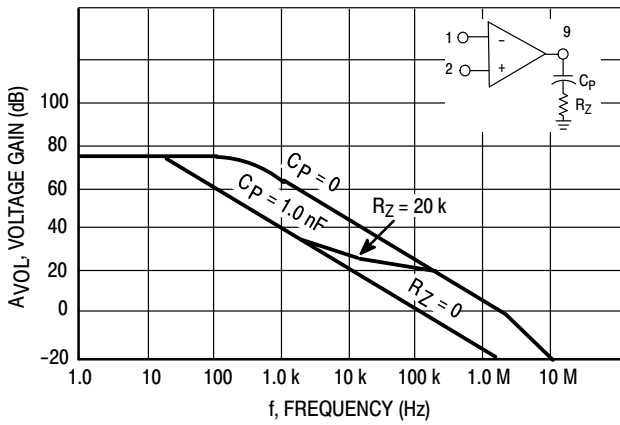


Figure 5. Error Amplifier Open Loop Frequency Response

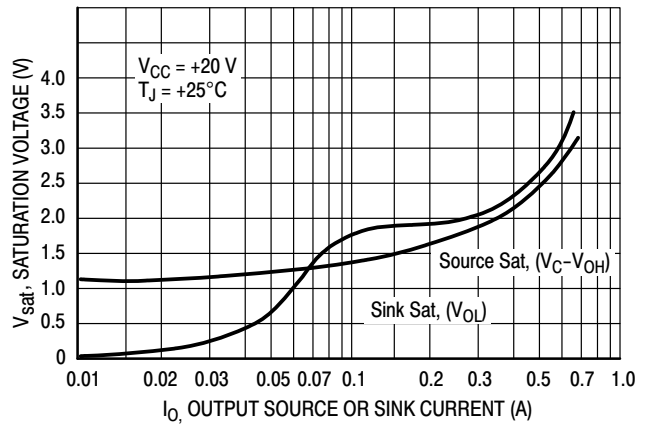


Figure 6. Output Saturation Characteristics

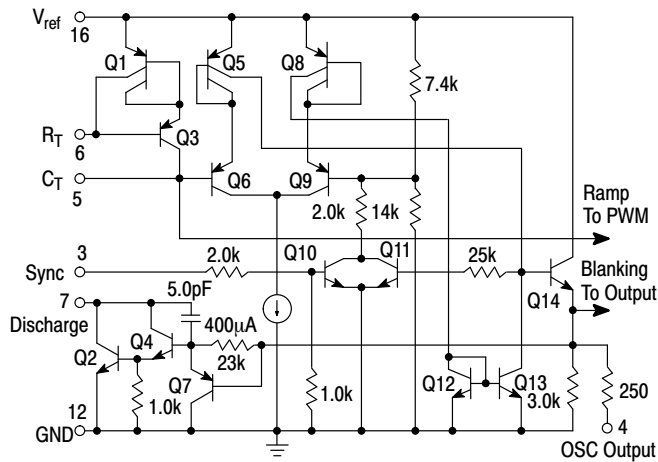


Figure 7. Oscillator Schematic

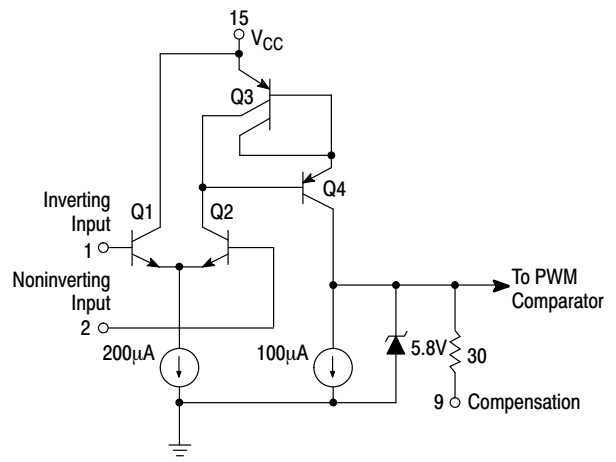


Figure 8. Error Amplifier Schematic

SG3525A

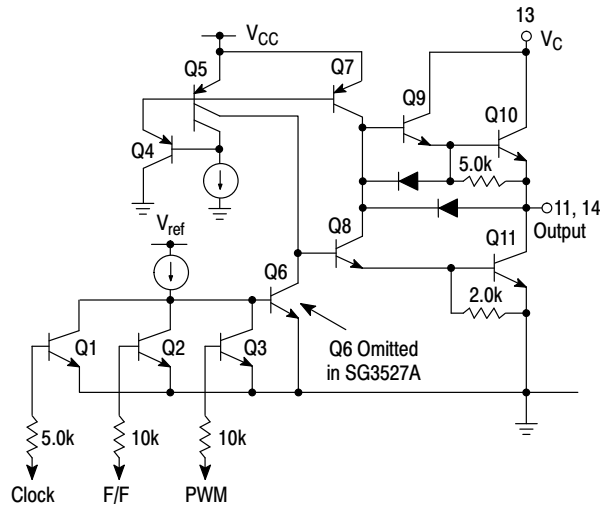
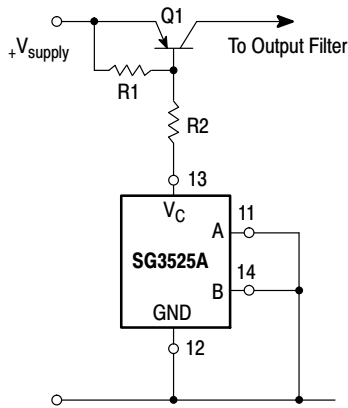
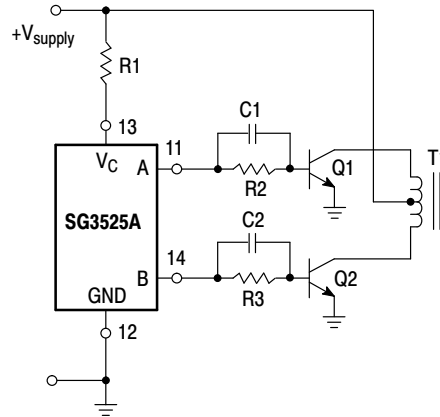


Figure 9. Output Circuit
(1/2 Circuit Shown)



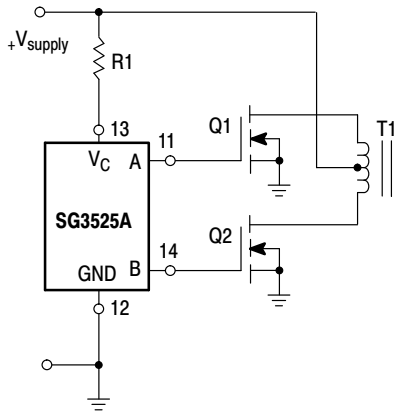
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 10. Single-Ended Supply



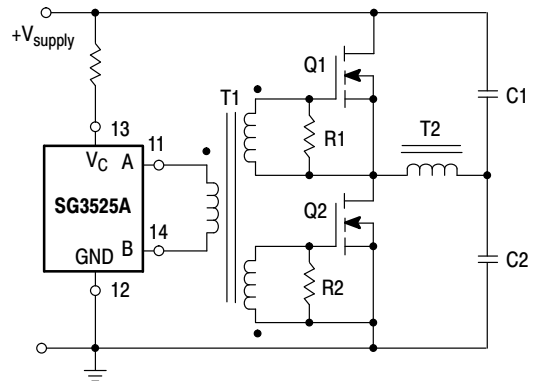
In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

Figure 11. Push-Pull Configuration



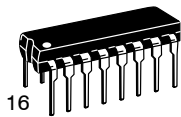
The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

Figure 12. Driving Power FETS



Low power transformers can be driven directly by the SG3525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

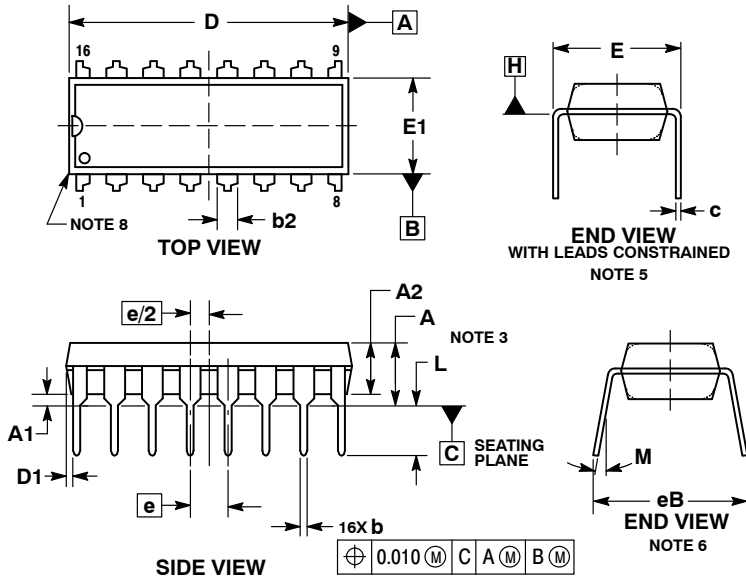
Figure 13. Driving Transformers in a Half-Bridge Configuration



SCALE 1:1

PDIP-16
CASE 648-08
ISSUE V

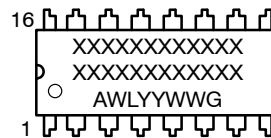
DATE 22 APR 2015



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
 4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
 5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
 6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
 7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
 8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 0.210 | --- | 5.33 |
| A1 | 0.015 | --- | 0.38 | --- |
| A2 | 0.115 | 0.195 | 2.92 | 4.95 |
| b | 0.014 | 0.022 | 0.35 | 0.56 |
| b2 | 0.060 TYP | | 1.52 TYP | |
| C | 0.008 | 0.014 | 0.20 | 0.36 |
| D | 0.735 | 0.775 | 18.67 | 19.69 |
| D1 | 0.005 | --- | 0.13 | --- |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| eB | --- | 0.430 | --- | 10.92 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| M | --- | 10° | --- | 10° |

GENERIC
MARKING DIAGRAM*



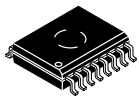
- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

- | | |
|----------------|---------------------|
| STYLE 1: | STYLE 2: |
| PIN 1. CATHODE | PIN 1. COMMON DRAIN |
| 2. CATHODE | 2. COMMON DRAIN |
| 3. CATHODE | 3. COMMON DRAIN |
| 4. CATHODE | 4. COMMON DRAIN |
| 5. CATHODE | 5. COMMON DRAIN |
| 6. CATHODE | 6. COMMON DRAIN |
| 7. CATHODE | 7. COMMON DRAIN |
| 8. CATHODE | 8. COMMON DRAIN |
| 9. ANODE | 9. GATE |
| 10. ANODE | 10. SOURCE |
| 11. ANODE | 11. GATE |
| 12. ANODE | 12. SOURCE |
| 13. ANODE | 13. GATE |
| 14. ANODE | 14. SOURCE |
| 15. ANODE | 15. GATE |
| 16. ANODE | 16. SOURCE |

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|------------------|-------------|--|
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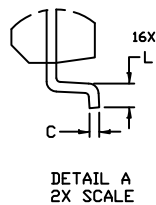
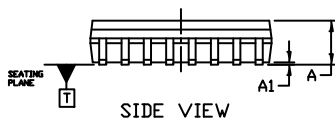
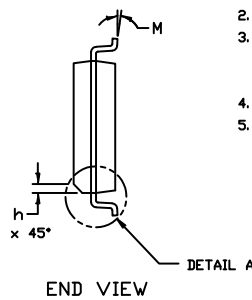
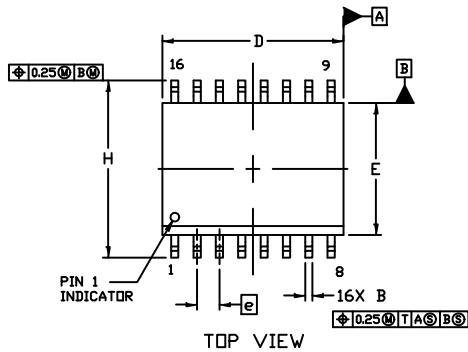
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1
SCALE 1:1

SOIC-16 WB
CASE 751G
ISSUE E

DATE 08 OCT 2021

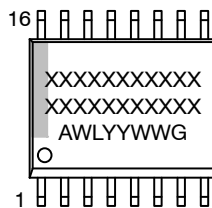


NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
- MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

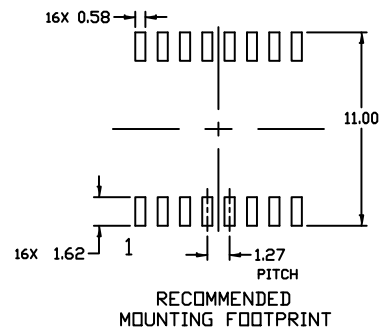
| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN. | MAX. |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.53 REF | |
| L | 0.50 | 0.90 |
| M | 0° | 7° |

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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